Real-time Ethernet, Multi-protocol (REM) Switch

2 – Port, Embedded Switch with High-Throughput Processor Interface

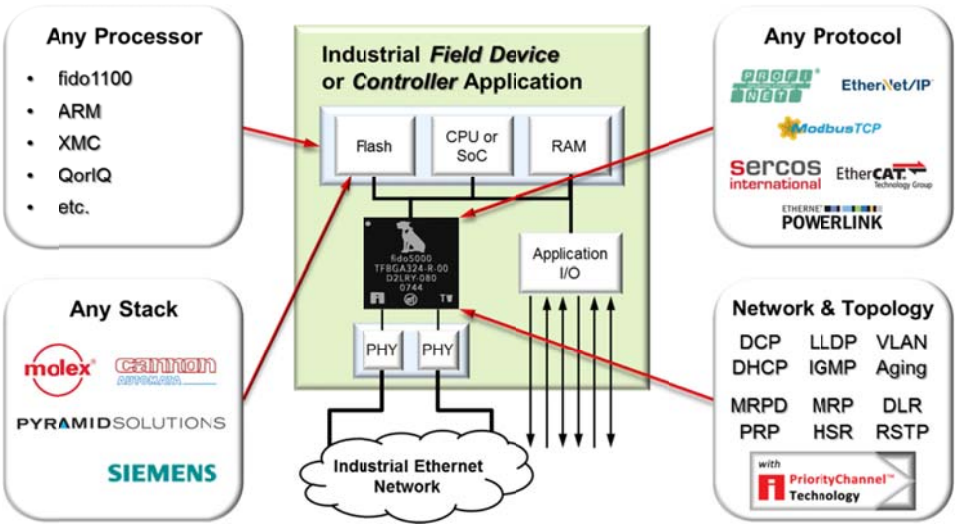
The fido5000 REM Switch supports all major Industrial Ethernet protocols and connects to any processor to build any field device or controller application

The REM Switch is a 2-Port embedded Ethernet switch that interfaces to any processor including any ARM® CPU and Innovasic's fido1100® Communication Controller. Innovasic's PriorityChannel™ Technology has been integrated into the switch's hardware architecture and designed into the REM switch software drivers. The protocols supported are PROFINET Class C (IRT) and Class B (RT), EtherNet/IP with and without DLR, ModbusTCP, EtherCAT, SERCOS, and POWERLINK. The REM switch comes with a software driver for each protocol. The software drivers provide an API for integration with any field device or controller protocol stack. Innovasic is certifying REM and its software drivers at each protocol's sponsoring industry organization using Innovasic's RapID Platform.

Your processor, your stacks, one switch – amazing performance

The REM switch is designed so you can choose the type of processor that fits your application and not be forced to use a particular vendor's protocol stack. REM attaches to the memory bus of a processor and looks like any other peripheral out on that bus. The memory cycle for REM goes down to 32 ns (125 Mbytes/second with a 32-bit bus) to support the 12.5 µs cycle time for EtherCAT and the 31.25 µs cycle time for PROFINET IRT. Data is transferred to and from the switch using PriorityChannel™ queues so real-time data transfers can interrupt non real-time data transfers without delay. These queues are managed by the switch driver and interface to the protocol stack to achieve the most efficient data transfers possible. This also means the application software doesn't have to worry about managing the switch, setting low-level registers, or keeping track of intricate time management processes.

Another performance advantage of the REM switch is that its PriorityChannel™ Technology makes it immune to network loading effects. This advantage ensures your application is up and running all the time, every time. The REM switch intelligently filters packets to keep unwanted traffic from your processor, manage low priority traffic based on the loading of your processor, and guarantee the timely delivery of high priority packets regardless of overall packet load.



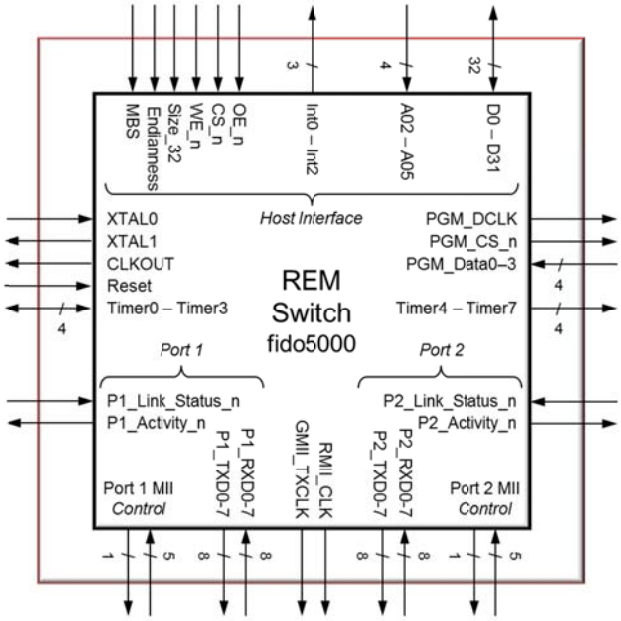
Innovasic®

www.innovasic.com

Real-time Ethernet, Multi-protocol (REM) Switch

2 – Port, Embedded Switch with High-Throughput Processor Interface

Flexible hardware integration



The REM switch is divided into three major functional blocks: The Host Interface, Time Control Unit (TCU), and Ethernet Interface. The Host Interface is a high-throughput memory interface that can be configured to either 16- or 32-bits, use multiplexed or separate address and data, and select the data format to either Big Endian or Little Endian data order. Three interrupt lines are configured by the software driver to prioritize communication between the REM switch and the processor.

The core of the TCU functionality is a sophisticated counter that is synchronized and syntonized with the protocol-specific synchronization master. The counter controls time-specific network events and signals the host processor with respect to synchronous I/O actions. In addition, there are 4 input-capture/output-compare units that can be used to timestamp or generate external events based on the same counter. A user application on the host processor can use the REM driver to create periodic waveforms on REM outputs to control external devices (e.g. start an ADC at a precise time), control host processor actions (interrupts, DMA operations, etc.) or synchronize the host processor with REM.

The Ethernet Interface is two ports and each port can be configured for either RMII, MII, or GMII to support IEEE 802.3, 10/100/1000 Mb/s, Half and Full Duplex, IPv6 and IPv4 communication. This allows the user to select any PHY to suit the particular application. PHY configuration is direct from the processor to the PHYs' MDIO interface to provide maximum flexibility. The MII interface is recommended for applications requiring the lowest jitter and latency. The Link Activity output drives an LED to indicate a link is valid.

Simplified software integration

The software drivers include a standard set of interfaces to support standard, low priority, TCP/IP communications, basic switch initialization, timer configuration, and interrupt management. This interface is common to all REM switch drivers, easing the porting of your application to each supported protocol. Each protocol has its own interface that configures the REM switch for optimal operation. This configuration is transparent to the user and can be performed at any time including a soft-boot to change protocols without resetting the host processor or PHYs. Configuration takes less than 150 ms in order to support Fast Start-Up for PROFINET and QuickConnect for EtherNet/IP.